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10/561,270	01/23/2006	Hirobumi Furihata	074273-0242	5886

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,270	FURIHATA ET AL.	
	Examiner	Art Unit	
	VINH LAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *4,5,13-18,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-12,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims **1-3**, **6-12**, and **19** are rejected under 35 U.S.C. 102(e) as being anticipated by **Nose et al. (US Patent No. 7206003)**.

Regarding Claim **1**, (Currently Amended) **Nose et al.** teach a controller/driver comprising:

a work memory *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. first display memory **7a**; Col. **8**, Ln. **3-11**, i.e. a part of the partitioned display memory is used as, for example, a memory*

area for storing corrected image data, a drawing memory area for using a graphic function, a memory area for storing overdrive data for performing overdrive processing);

a graphic engine *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. memory control circuit **6**)* converting externally received image data *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. 8-bit data from **1**; a memory control circuit 6 for controlling the display memories with a display memory control signal; Col. **9**, Ln. **13-20**, i.e. image data is stored at an address specified by the display memory control signal)* into first bitmap data *(Col. **9**, Ln. **27-34**, FIG. **1**, i.e. higher order 4 bits)*, and storing said first bitmap data into said work memory *(Col. **9**, Ln. **27-34**, FIG. **1**)*;

a display memory *(Col. **9**, Ln. **35-41**, FIG. **1**, i.e. second selector **9**; Col. **9**, Ln. **66-67**, Col. **10**, Ln. **1-9**, FIG. **3**, i.e. second selector 9 controlled according to the memory read select signal selects the image data stored in the first display memory 7a… the high order 4 bits of the above image data read from the first display memory… transferred to… latch circuit 12)* receiving and storing second bitmap data developed from said first bitmap data stored in said work memory *(Col. **9**, Ln. **35-41**, FIG. **1**, i.e. second selector **9** transferring data from **7a** to **12**)*; and

a driver circuit *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. data line drive circuit **13**)* which receives said second bitmap data from said display memory, and drives, a display panel in response to said second bitmap data received from said display memory *(Col. **8**, Ln. **45-68**, FIG. **1**)*,

wherein said first bitmap data includes a plurality of line data each including a plurality of pixel data associated with a line of pixels of an image represented by said

second bitmap data to be displayed on said display panel *(Col. **9**, Ln. **41-44**, FIG. **1**, i.e. **Hx4bit**)*, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is performed *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. inherently because it's indicative of gate line drive circuit **5** with a timing control signal)* such that each of said plurality of line data is transferred at the same time in parallel from said work memory to said display memory *(FIG. **3**, i.e. inherently because it's indicative of transferring **Hx4bit** data in parallel from **7a** to **12**)*.

Regarding Claim **2**, (Original) **Nose et al.** teach the controller/driver according to claim 1, wherein said image data is described in a vector format *(Col. **2**, Ln. **8-11**, i.e. image file).*

Regarding Claim **3**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 1, wherein said image data includes compressed image data *(Col. **2**, Ln. **8-11**, i.e. image file)*.

Regarding Claim **6**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 1, further comprising:

a latch receiving said line data from said work memory, and temporally storing said received line data *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. latch **12**).*

Regarding Claim **7**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 1, further comprising:

a timing controller *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. timing control circuit **11**)* controlling said work memory, said display memory, and said driver circuit so that said

data transfer of said first bitmap data from said work memory to said display memory *(Col. **8**, Ln. **45-68**, FIG. **1**)* is synchronous with readout of said second bitmap data from said display memory to said driver circuit *(FIG. **3**, i.e. inherently because it's indicative of transferring 4 bits data in parallel from **7a** to **12**)*; and

a memory controller *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. memory control circuit **6**)* connected to said second input port *(FIG. **1**, i.e. display memory control signal)* of said work memory, said memory controller receiving bit map data from a processor for storage in said display memory *(Col. **8**, Ln. **45-68**, FIG. **1**)*.

Regarding Claim **8**, (Original) **Nose et al.** teach the controller/driver according to claim 7, wherein said data transfer of said first bitmap data from said work memory to said display memory is initiated in response to activation of a frame synchronization signal indicating to start displaying each image frame *(Col. **8**, Ln. **45-68**, FIG. **1**)*.

Regarding Claim **9**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 7, wherein said timing controller controls said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory does not overrun said readout of said second bitmap data from said display memory to said driver circuit *(FIG. **3**, i.e. inherently because it's indicative of transferring 4 bits data in parallel from **7a** to **12**)*.

Regarding Claim **10**, (Original) **Nose et al.** teach the controller/driver according to claim 1, wherein said work memory includes:

a plurality of first bit lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits, 12, and 13)*,

a plurality of first word lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits, 12, and 13)*, and

a plurality of first memory cells disposed at respective intersections of said first bit lines and first word lines to store therein said first bitmap data *(Col. **9**, Ln. **60-61**, FIG. **3**, i.e. high order 4 bits "**1100**" of **7a**)*,

wherein said display memory includes:

a plurality of second bit lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits, 12, and 13)*,

a plurality of second word lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits, 12, and 13)*, and

a plurality of second memory cells disposed at respective intersections of said second bit lines and second word lines to store therein said second bitmap data *(Col. **9**, Ln. **60-61**, FIG. **3**, i.e. high order 4 bits "**1100**" output of **9**)*,

wherein a number of said first bit lines is same as that of said second bit lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits)*, and

wherein said first bit lines are connected to said second bit lines, respectively *(FIG. **1**)*.

Regarding Claim **11**, (Original) **Nose et al.** teach the controller/driver according to claim 10, wherein a number of said first word lines is identical to that of said second word lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits)*.

Regarding Claim **12**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 10, further comprising a timing controller *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. timing control circuit **11**)* controlling said work memory *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. first display memory **7a**)*, and said display memory *(Col. **9**, Ln. **35-41**, FIG. **1**, i.e. second selector **9**)*, and said driver circuit *(Col. **8**, Ln. **45-68**, FIG. **1**)*,

wherein said driver circuit is connected to said second bit lines *(FIG. **1**)*, and

wherein said timing controller *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. timing control circuit **11**)* is adapted to deactivate *(FIG. **5**, i.e. Second Selector Output shown in dashed line (Memory Read Select Signal (Select2) Off; Col. **8**, Ln. **45-68**, i.e. memory control circuit 6 for controlling the display memories with a display memory control signal and controlling the selectors with a memory partition signal; therefore the selector would not select ("deactivated") since both Memory Partition Signal (Select 1) and Memory Read Select Signal (Select 1) are OFF)* said display memory *(Col. **9**, Ln. **35-41**, FIG. **1**, i.e. second selector **9**)* to allow said first bitmap data *(Col. **9**, Ln. **27-34**, FIG. **1**, i.e. higher order 4 bits)* to be transmitted from said work memory *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. first display memory **7a**)* to said driver circuit *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. data line drive circuit **13**)* through said second bit lines *(Col. **9**, Ln. **14-20**, FIG. **1**, i.e. H pixels x V pixels x 4bits, 12, and 13)*.

Regarding Claim **19**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 1, further comprising:

a latch receiving said first bitmap data from said work memory, and temporally storing said first bitmap data *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. latch **12**)*; and

a timing controller *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. timing control circuit **11**)* for controlling output of data from said latch, wherein said display memory receives said first bitmap data output from said latch *(Col. **8**, Ln. **45-68**, FIG. **1**)*,

wherein said work memory and said display memory are operated at different times due to having said latch provided therebetween *(Col. **8**, Ln. **45-68**, FIG. **1**)*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim **20** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nose et al. (US Patent No. 7206003)** in view of **Patrick et al. (US Patent No. 5644758).**

Regarding Claim **20**, (Previously Presented) **Nose et al.** teach the controller/driver according to claim 1, further comprising:

means for transferring said first bitmap data from said work memory to said display memory *(Col. **8**, Ln. **45-68**, FIG. **1**)*; and

means for displaying said second bitmap data output from said display memory on said display panel *(Col. **8**, Ln. **45-68**, FIG. **1**)*.

However, **Nose et al.** do not teach a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel.

In the same field of endeavor, **Patrick et al.** further teach a first rate at which said first bitmap data *(i.e. image data blocks that are not color, text, and graphics)* is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data *(i.e. image data blocks that comprise color, text, and graphics…slower rate)* is output from said display memory for display on said display panel (Col. **2**, Ln. **1**-**10**).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Nose et al.** teaching of a controller/driver comprising of the graphic engine, work memory, display memory, driver circuit, and of connections among the graphic engine, work memory, display memory, and driver circuit with **Patrick et al.** teaching of a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel *to reduce the power consumption and latency of a display*.

Response to Arguments/Amendments/Remarks

3. Claims **4**-**5** and **18** are canceled.

4. Claims **13-17** are withdrawn.

5. Newly added Claims **21** and **22** are directed toward *Non-Elected Species 3*.

6. Applicant's arguments filed 03/09/2011 have been fully considered but they are not persuasive.

First of all concerning Claim **1**, applicant argues that:

(i) On Page 9, **Nose et al.**'s first display memory 7a is not a work memory. However, the Examiner respectfully disagrees because:

(a) There is no claimed limitation that is *specifically and structurally differentiated* between the "*first display memory 7a"* and "*work memory"* other than naming preference.

(b) **Nose et al.** explicitly discloses that "…*a part of the partitioned display memory is used as, for example, a memory area for storing corrected image data, a drawing memory area for using a graphic function, a memory area for storing overdrive data for performing overdrive processing" (Col. **8**, Ln. **3-11**).*

(ii) On Page 9, **Nose et al.**'s memory control circuit 6 does not operate as a graphic engine since no image data is provided to the memory control circuit 6. However, the Examiner respectfully disagrees because:

(a) The memory control circuit 6 *must receive image data* so that image data would be evenly divided into High and Low Order 4-bit corresponding to the correct First and Second Displays *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. 8-bit data from **1**; a memory control*

*circuit 6 for controlling the display memories with a display memory control signal; Col. **9**, Ln. **13-20**, i.e. image data is stored at an address specified by the display memory control signal).*

(b) The Examiner broadly interprets "image data" comprises not only gradation data but also control and timing data for synchronization so that the desired images would have been produced sequentially and orderly.

(iii) On Page 9, **Nose et al.**'s second selector 9 does not operate as a display memory. However, the Examiner respectfully disagrees because:

(a) *Second Selector **9*** operates identically to The First Display Memory 7a since *Second Selector **9*** receives (or to be ***written***) to the *current-frame* High Order 4 bits Image Data which must be remained (or to be ***stored***) in *second selector **9*** for a predetermined period of time. The *current-frame* High Order 4 bits Image Data is not transferred to the Latch Circuit 12 until the *next-frame* High Order 4 bits Image Data are written into the First Display Memory 7a because of synchronization between frames *(Col. **9**, Ln. **35-41**, FIG. **1**, i.e. second selector **9**; Col. **9**, Ln. **66-67**, Col. **10**, Ln. **1-9**, FIG. **3**, i.e. second selector 9 controlled according to the memory read select signal selects the image data stored in the first display memory 7a… the high order 4 bits of the above image data read from the first display memory… transferred to… latch circuit 12).*

(b) The *Second selector **9*** not only operates identically to The First Display Memory 7a but also is used to *select* either the High or Low Order 4 bits Image Data

from the corresponding First or Second Display Memories (7a or 7b respectively) hence the name is suggested as such.

Secondly concerning Claim **12** (Page 10), applicant argues that **Nose et al.** do not teach "…*said timing controller is adapted to deactivate said display memory*…" since the "…dashed lines provided in the top row of that figure show that no data is provided...". However, the Examiner respectfully disagrees because **Nose et al.** teach

wherein said timing controller *(Col. **8**, Ln. **45-68**, FIG. **1**, i.e. timing control circuit **11**)* is adapted to deactivate *(FIG. **5**, i.e. Second Selector Output shown in dashed line (Memory Read Select Signal (Select2) Off; Col. **8**, Ln. **45-68**, i.e. memory control circuit 6 for controlling the display memories with a display memory control signal and controlling the selectors with a memory partition signal; therefore the selector would not select ("deactivated") since both Memory Partition Signal (Select 1) and Memory Read Select Signal (Select 1) are OFF)* said display memory *(Col. **9**, Ln. **35-41**, FIG. **1**, i.e. second selector **9**).*

Finally concerning Claim **20** (Pages 10-11), applicant argues that **Patrick et al.** "would appear to teach having a *same* fast transfer rate between all of the devices in his display system". However, the Examiner respectfully disagrees because **Patrick et al.** teach

a first rate at which said first bitmap data *(i.e. image data blocks that are not color, text, and graphics)* is transferred from said work memory to said display memory

is faster than a second rate at which said second bitmap data *(i.e. image data blocks that comprise color, text, and graphics…slower rate)* is output from said display memory for display on said display panel (Col. **2**, Ln. **1**-**10**).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH T. LAM whose telephone number is (571)270-3704. The examiner can normally be reached on M-F (7:00-4:30) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vinh T Lam/
Examiner, Art Unit 2629

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629